SQUAREHEAD TECHNOLOGY

THE TWO MEMORY MODELS

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C++ UNDER THE SEA 2025

Squarehead / CppQuiz.org

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CPPQUIZ.ORG

C++ Quiz

You've answered 0 of 178 questions correctly. (Clear)

Question #197 Difficulty: ●○○

According to the C++23 standard, what is the output of this program?

```
#include <iostream>

int j = 1;

int main() {
  int& i = j, j;
  j = 2;
  std::cout << i << j;
}
```

Answer: The program is guaranteed to output: Answer

Problems? View a hint or try another question.

I give up, show me the answer (make 3 more attempts first).

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The Pragmatic Programmers

C++ Brain Teasers

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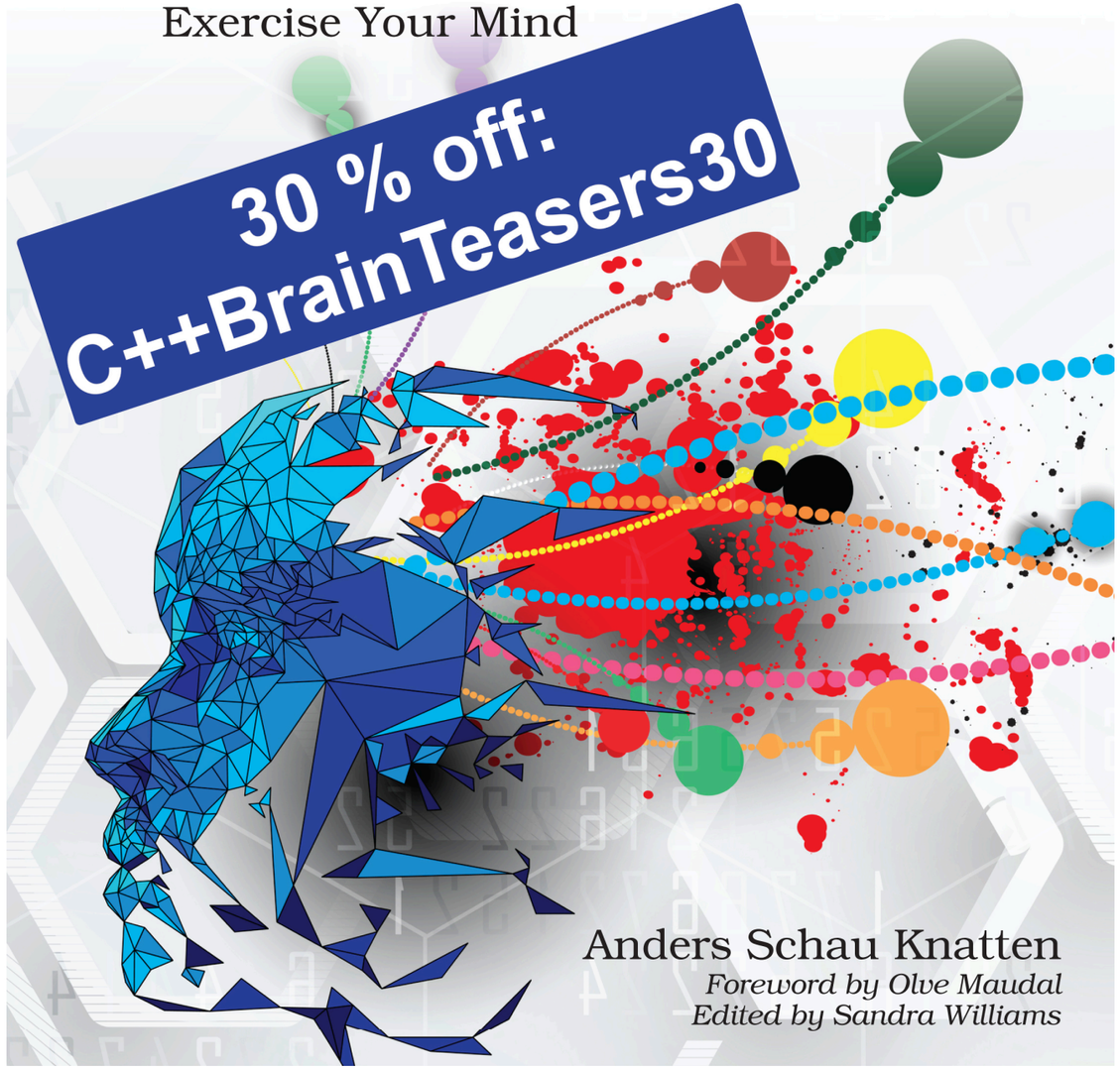

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THE TWO MEMORY MODELS

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- Why?

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- Why?
- Theoretical background

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- Why?
- Theoretical background
- Intuition, framework for reasoning

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THE TWO MEMORY MODELS

- Why?
- Theoretical background
- Intuition, framework for reasoning
- How stuff works!

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THE TWO MEMORY MODELS

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- High Level language (C++, C, Rust)

THE TWO MEMORY MODELS

- High Level language (C++, C, Rust)
- CPU / Architecture

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C++ MEMORY MODEL

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C++ MEMORY MODEL

6.7.1 Memory model [intro.memory]

1 The fundamental storage unit in the C++ memory model is the byte. A byte is at least large enough to contain any member of the execution character set ([lex.charset]) and the eight-bit code units of the Unicode[89] UTF-8 encoding form and is composed of a contiguous sequence of bits,[33] the number of which is implementation-defined. The least significant bit is called the *low-order bit*; the most significant bit is called the *high-order bit*. The memory available to a C++ program consists of one or more sequences of contiguous bytes. Every byte has a unique address.

2 A *memory location* is either an object of scalar type that is not a bit-field or a maximal sequence of adjacent bit-fields all having nonzero width. Two or more threads of execution can access separate memory locations without interfering with each other.

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- What's meant by "a memory location"
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C++ MEMORY MODEL

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  - Thread support library [thread]

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CPU MEMORY MODEL

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- X86, ARM, RISC-V, ...

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- "A memory consistency model is a set of rules specifying the values that can be returned by loads of memory." - RISC-V ISA manual

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CPU MEMORY MODEL

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WHAT HAS THE MEMORY MODEL EVER DONE FOR ME?

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- C++ memory model
  - Single threaded examples
  - Multi threaded example
  - Memory ordering

WHAT HAS THE MEMORY MODEL EVER DONE FOR ME?

- C++ memory model
  - Single threaded examples
  - Multi threaded example
  - Memory ordering
- CPU memory model:
  - Several variations, including x86 and RISC-V

SINGLE THREADED EXAMPLE

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```
1 int compute(const int* a, const int* b)
2 {
3     int result = *a;
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- Abstract machine
- Only need to emulate observable behaviour
- Observable: I/O, files, volatile, plus more implementation defined
- Can reorder

SINGLE THREADED EXAMPLE

```
1      // original                    // reordered
2      load reg_0, *a                 load reg_0, *a
3      add  reg_0, reg_0, 1           load reg_1, *b
4      load reg_1, *b                 add  reg_0, reg_0, 1
5      add  reg_0, reg_0, reg_1       add  reg_0, reg_0, reg_1
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- Can we swap the order of the loads too?

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```

- Or CPU reorders it on the fly
- "All" modern CPUs are out-of-order
- Can we swap the order of the loads too?
- Yes, can't affect the observable behaviour

SINGLE THREADED EXAMPLE (X86)

GCC 15.1 –03

```
int compute(const int* a, const int* b)
{
    int result = *a;
    result += 1;
    result += *b;
    return result;
}
```

```
1 compute(int const*, int const*):
2 mov     edx, DWORD PTR [rdi]
3 mov     eax, DWORD PTR [rsi]
4 lea     eax, [rdx+1+rax]
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SINGLE THREADED EXAMPLE 2

```
1 void compute(int* a, int* b)
2 {
3     int result = get_value();
4     result++;
5     *a = 2;
6     *b = result;
7 }
```

SINGLE THREADED EXAMPLE 2

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```

- Can we start the store to a earlier?

SINGLE THREADED EXAMPLE 2

```
1     // original
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SQUAREHEAD TECHNOLOGY

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Or CPU reorders it

CPU could reorder the stores!

SINGLE THREADED EXAMPLE 2

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move  reg_0, get_value()
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- C++ to CPU: Do not store a before calling get_value!

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- C++ to CPU: Do not store a before calling get_value!
- C++ to CPU: Do not reorder stores!

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- C++ to CPU: Do not store a before calling get_value!
- C++ to CPU: Do not reorder stores!
- How do we express this to the CPU?

SQUAREHEAD TECHNOLOGY

SINGLE THREADED EXAMPLE 2 (X86)

GCC 15.1 –03

```
void compute(int* a, int* b)
{
    int result = get_value();
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    *a = 2;
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}
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 1 compute(int*, int*):
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 3 mov     rbp, rdi
 4 push    rbx
 5 mov     rbx, rsi
 6 sub     rsp, 8
 7 call    get_value()
 8 mov     DWORD PTR [rbp+0], 2
 9 add     eax, 1
10 mov     DWORD PTR [rbx], eax
11 add     rsp, 8
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SQUAREHEAD TECHNOLOGY

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- X86 never reorders stores

SQUAREHEAD TECHNOLOGY

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- RISC-V **can** reorder stores

SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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```

- X86 never reorders stores
- RISC-V **can** reorder stores *to different addresses*
- Reorder includes effects from pipeline, caches, store buffers etc

SQUAREHEAD
TECHNOLOGY

MULTI THREADED EXAMPLE

SQUAREHEAD TECHNOLOGY

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MULTI THREADED EXAMPLE

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SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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- Informally: Always true

SQUAREHEAD TECHNOLOGY

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- Informally: Always true / always false (UB) / data race (UB)
- Forward progress: Terminate, I/O, volatile, or sync/atomic

SQUAREHEAD TECHNOLOGY

MULTI THREADED EXAMPLE (NON UB)

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1  Data data;
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6    add     rsp, 8
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11   test    al, al
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SQUAREHEAD TECHNOLOGY

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- Is the cache up to date?
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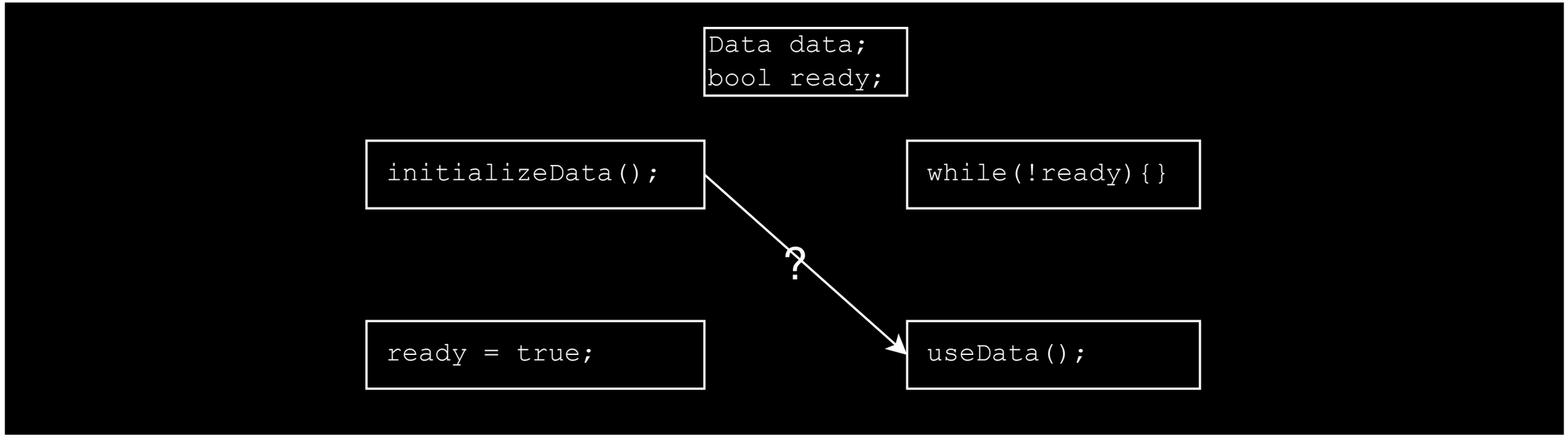

SQUAREHEAD
TECHNOLOGY

DATA RACE

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- Two expression evaluations conflict if **one of them modifies** a memory location and the **other one reads or modifies** the same memory location

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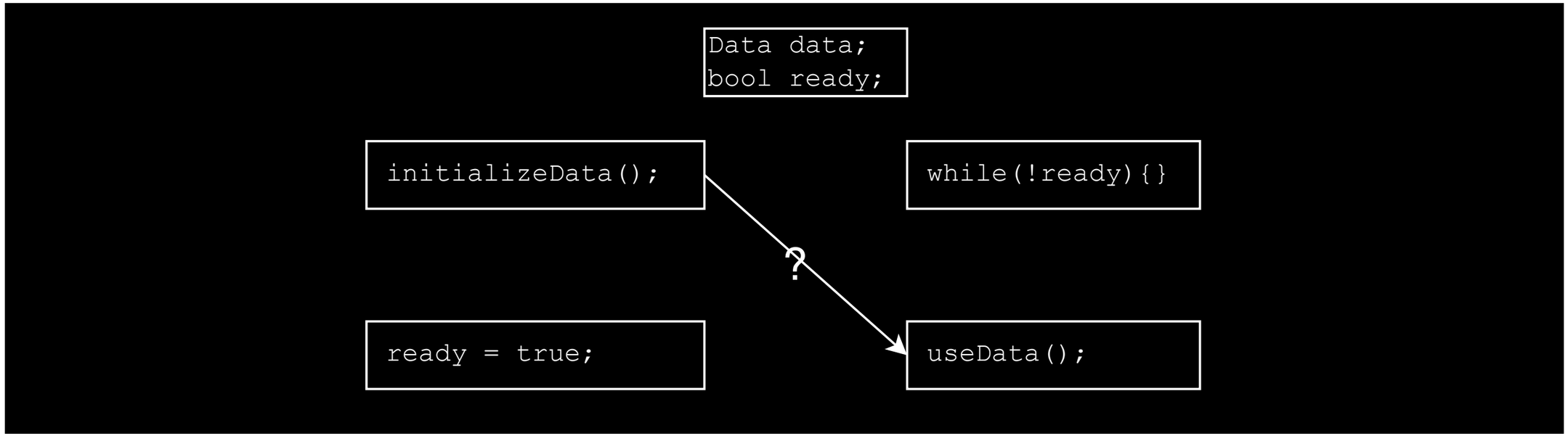
- The execution of a program contains a data race if it contains two potentially concurrent conflicting actions, at least one of which is not atomic, and **neither happens before the other**. Any such data race results in undefined behavior.
- Does the data write **happen before** the read?

SQUAREHEAD TECHNOLOGY

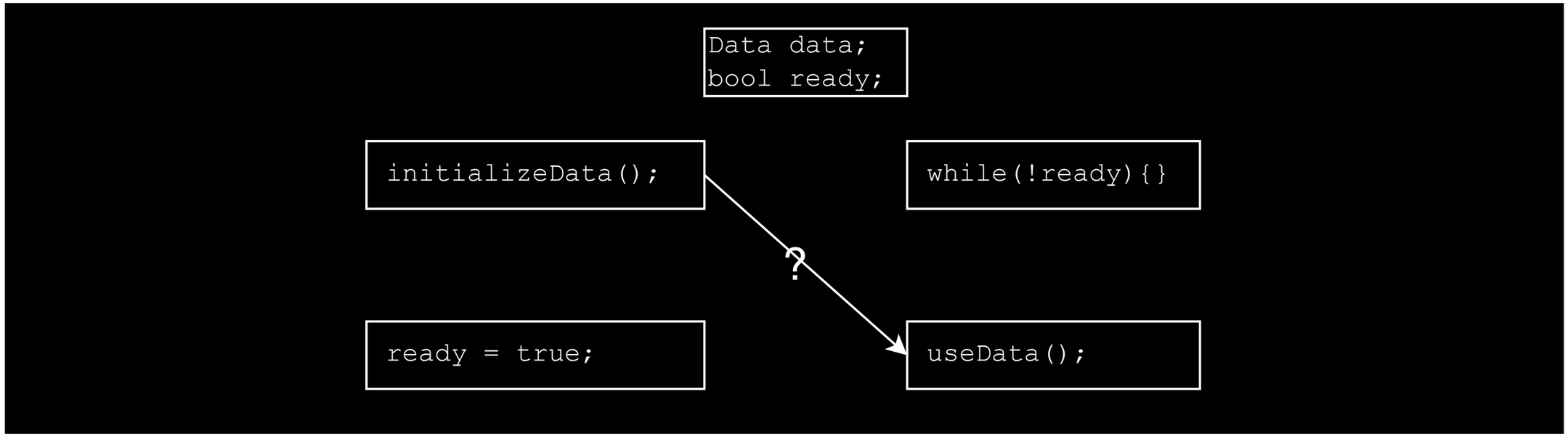
NON ATOMIC



Does `initializeData` **happen before** `useData`?

SQUAREHEAD TECHNOLOGY

NON ATOMIC

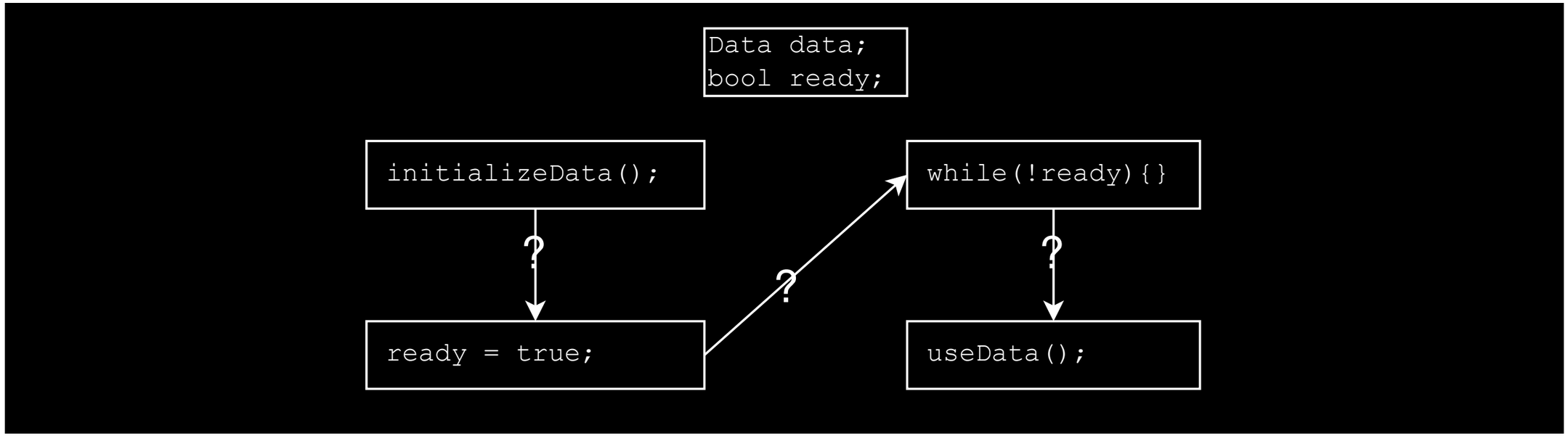


Does `initializeData` **happen before** `useData`?

Is there a *happens-before* relationship here?

SQUAREHEAD TECHNOLOGY

NON ATOMIC



SQUAREHEAD TECHNOLOGY

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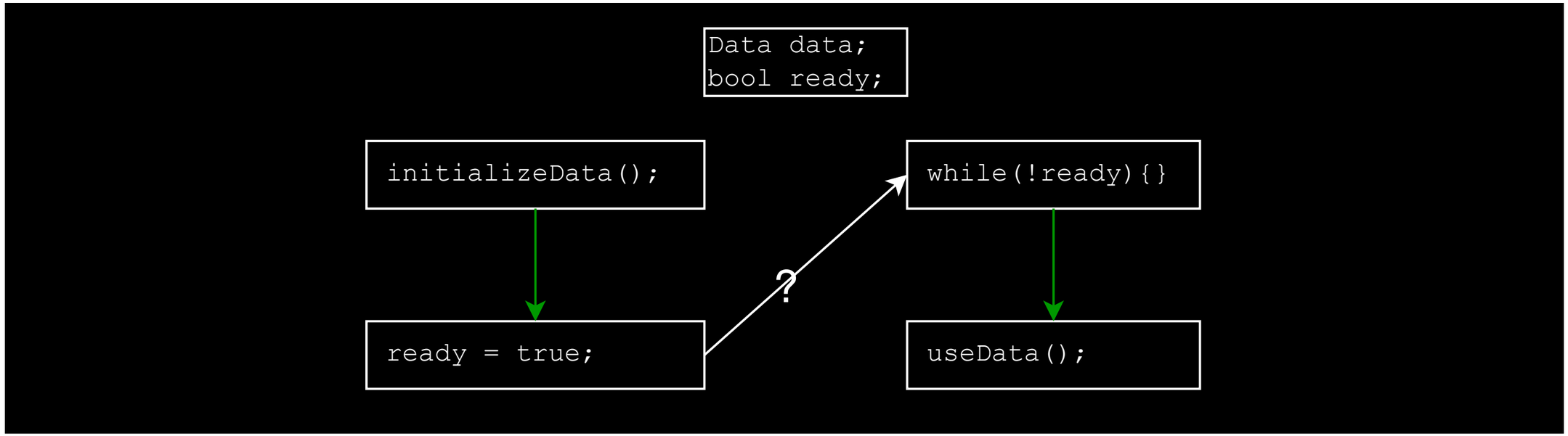

SQUAREHEAD TECHNOLOGY

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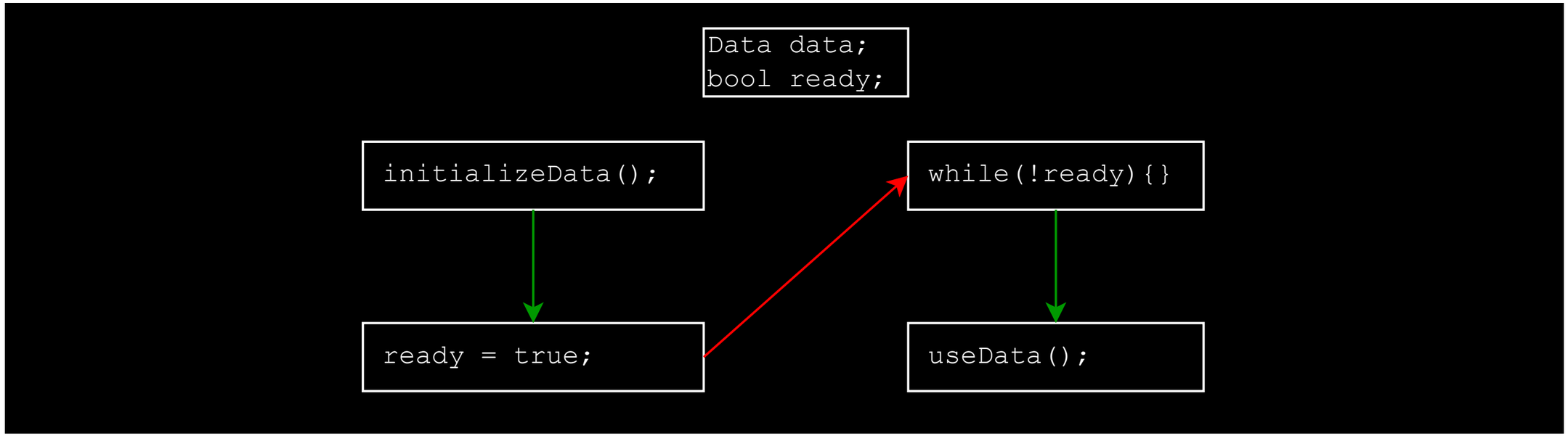

SQUAREHEAD TECHNOLOGY

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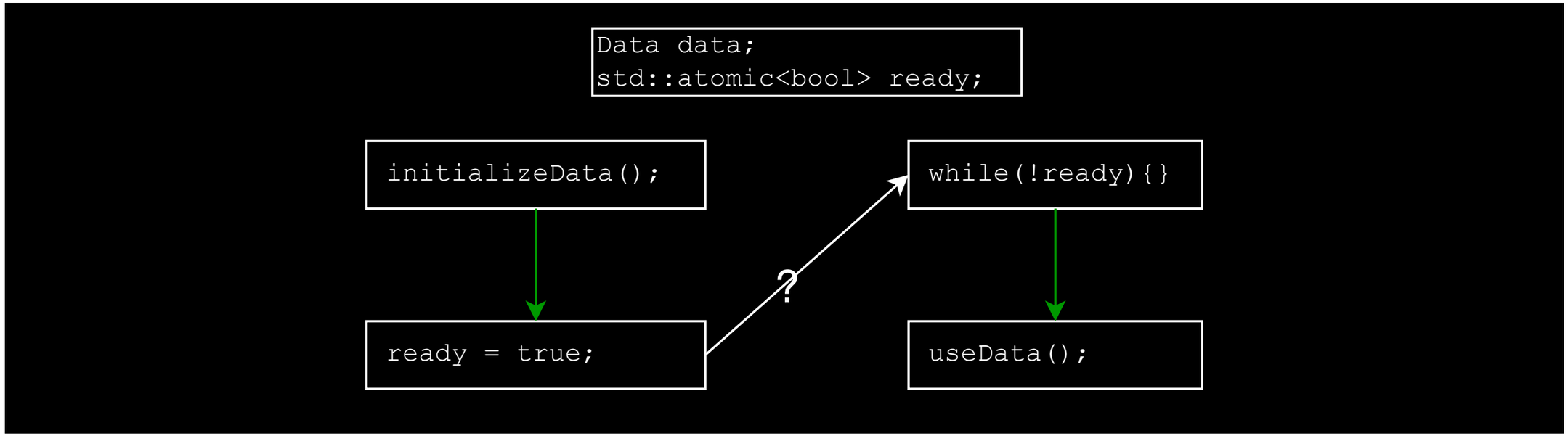

SQUAREHEAD TECHNOLOGY

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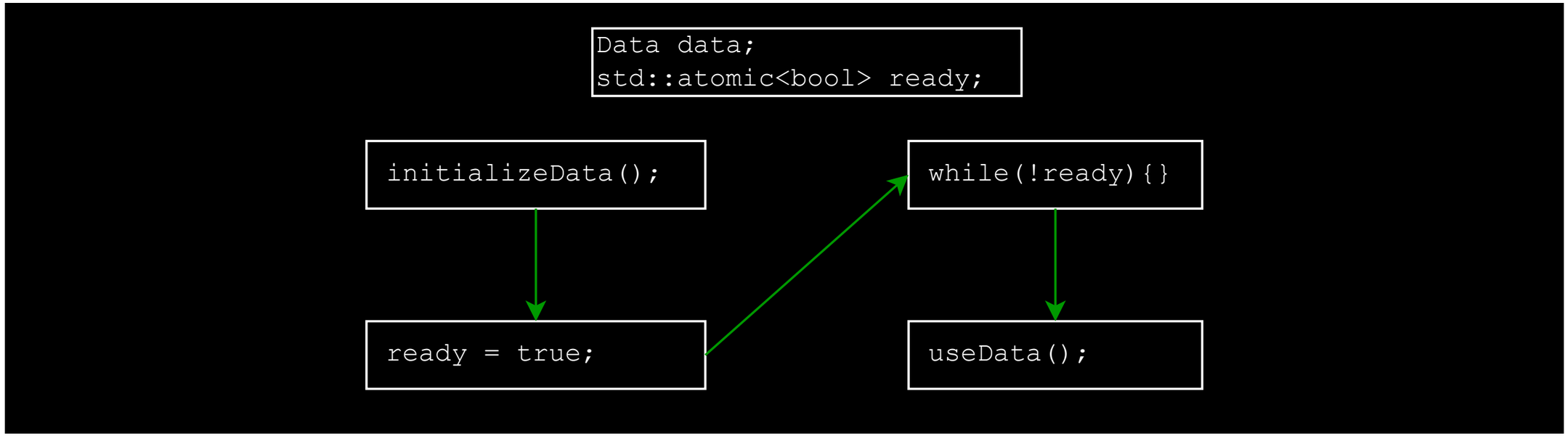

SQUAREHEAD
TECHNOLOGY

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- There is a total order to modifications of each *individual* atomic
- Otherwise, *it depends*

SQUAREHEAD TECHNOLOGY

MEMORY ORDER

```
Data data;
std::atomic<bool> ready{false};

void producer()
{
    initializeData();
    ready = true;
}

void consumer()
{
    while(!ready){}
    useData();
}
```

MEMORY ORDER

```
1  Data data;
2  std::atomic<bool> ready{false};
3
4  void producer()
5  {
6      initializeData();
7      ready.store(true, std::memory_order_seq_cst);
8  }
9
10 void consumer()
11 {
12     while(!ready.load(std::memory_order_seq_cst)){}
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SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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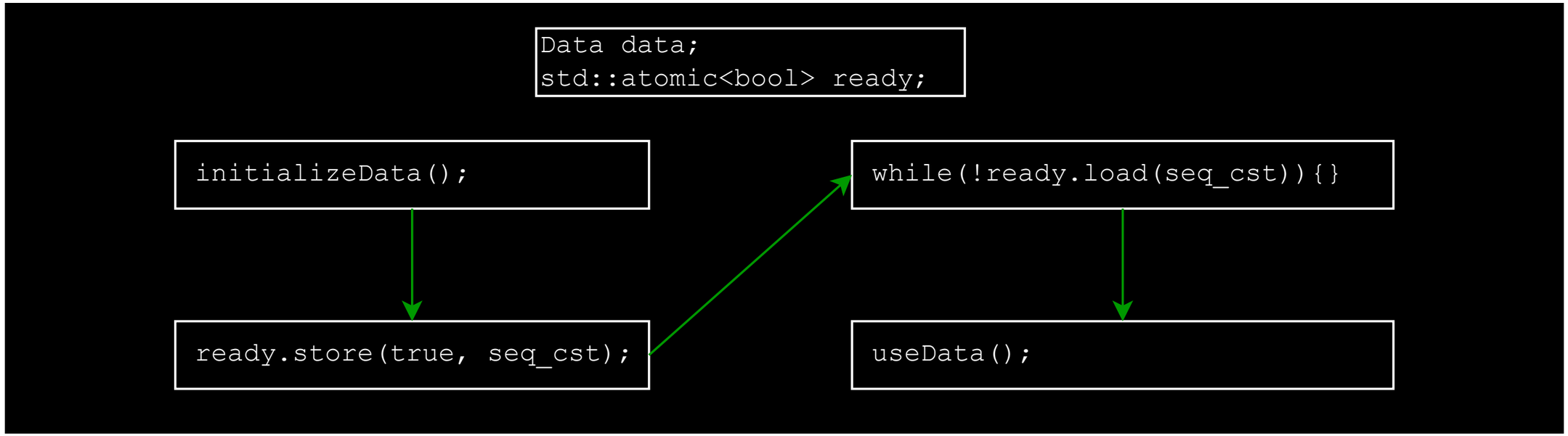
- Avoid half-written writes

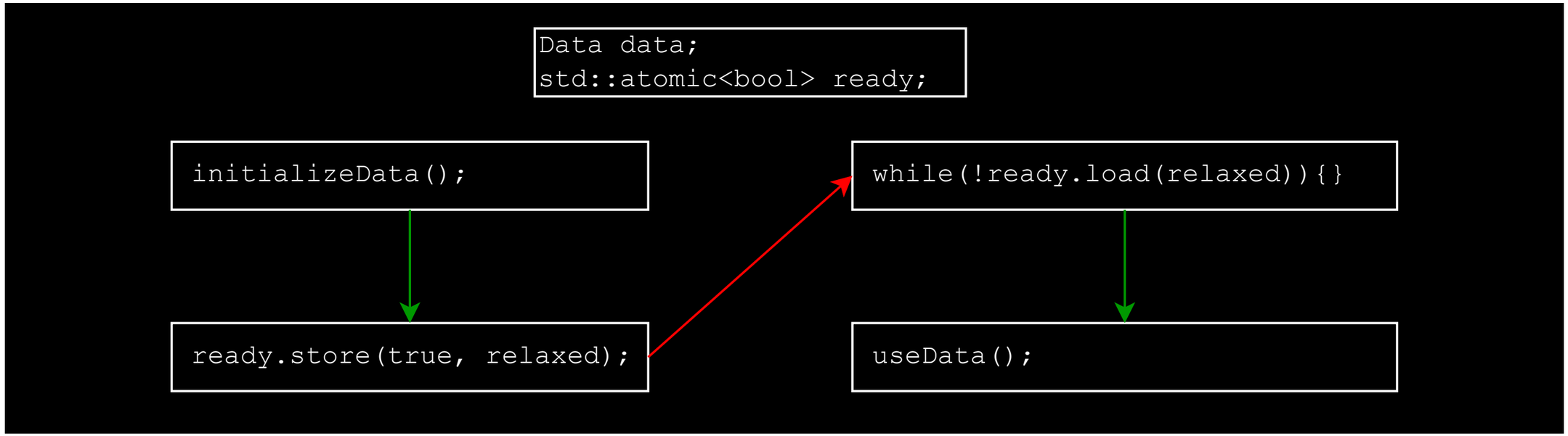
SQUAREHEAD TECHNOLOGY

SEQUENTIALLY CONSISTENT



SQUAREHEAD TECHNOLOGY

RELAXED

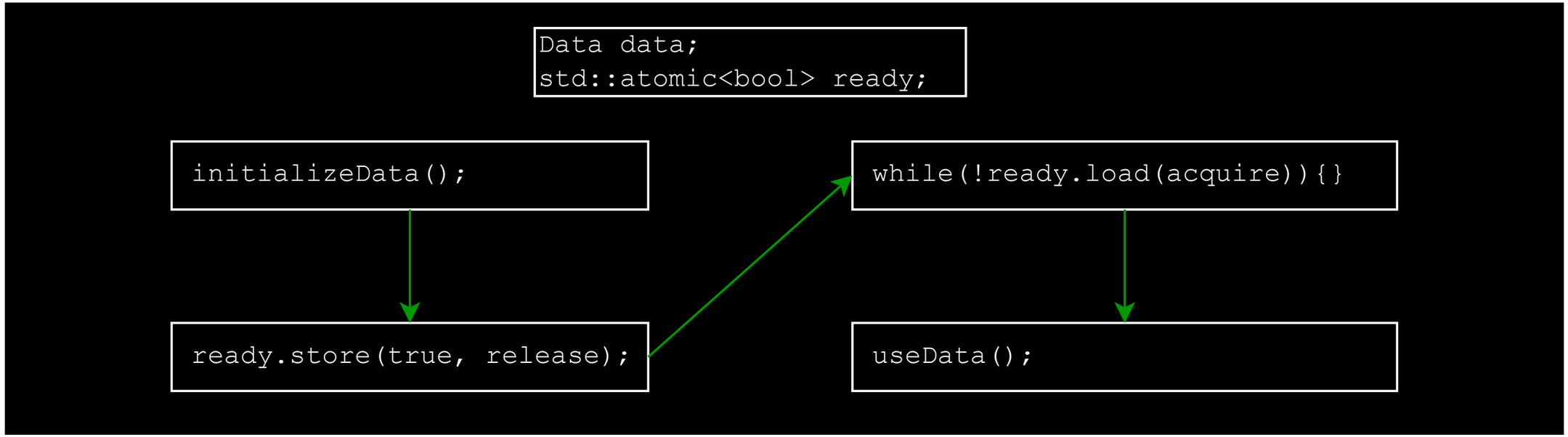


ACQUIRE / RELEASE

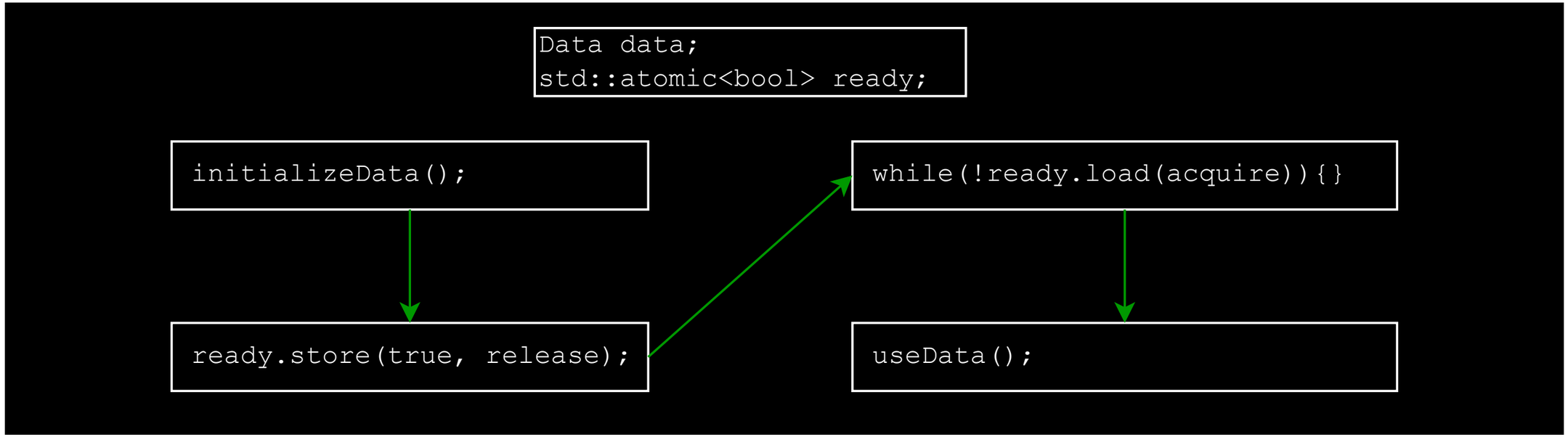
If an acquire-load observes the value of a release-store, the release-store happens before the acquire-load

SQUAREHEAD TECHNOLOGY

RELEASE/ACQUIRE



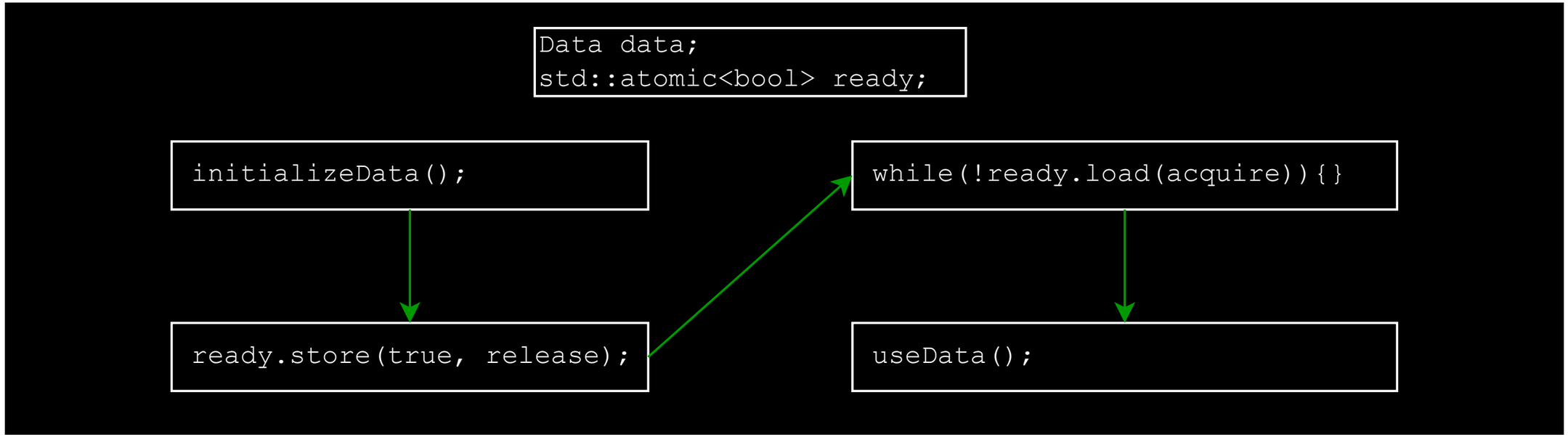
RELEASE/ACQUIRE



- Store happens-before load

SQUAREHEAD TECHNOLOGY

RELEASE/ACQUIRE



- Store happens-before load
- Can't reorder memory ops after the release-store

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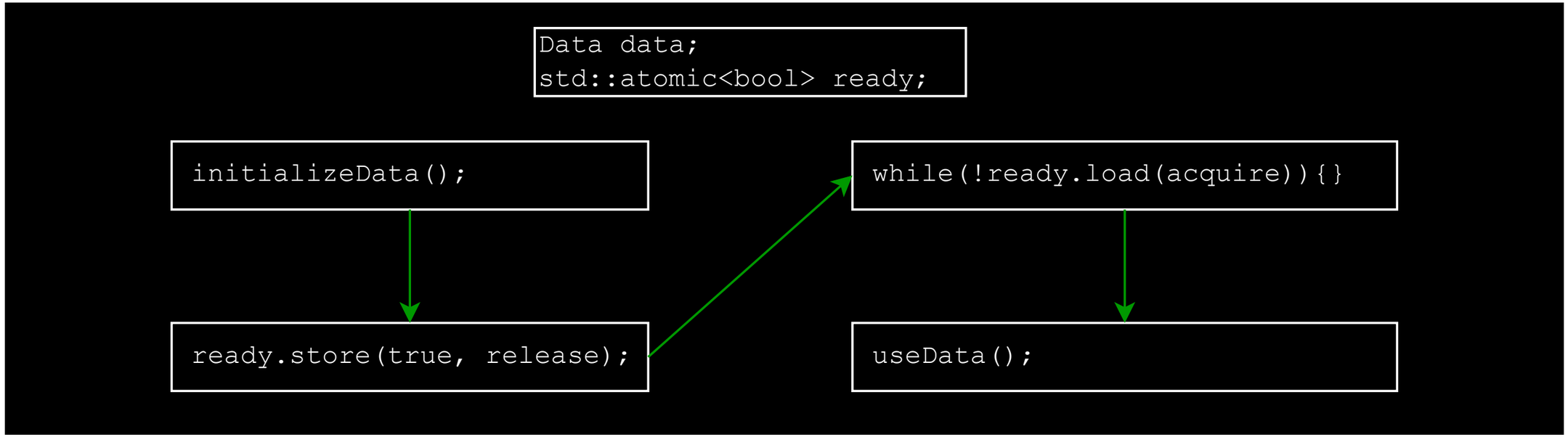

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SQUAREHEAD TECHNOLOGY

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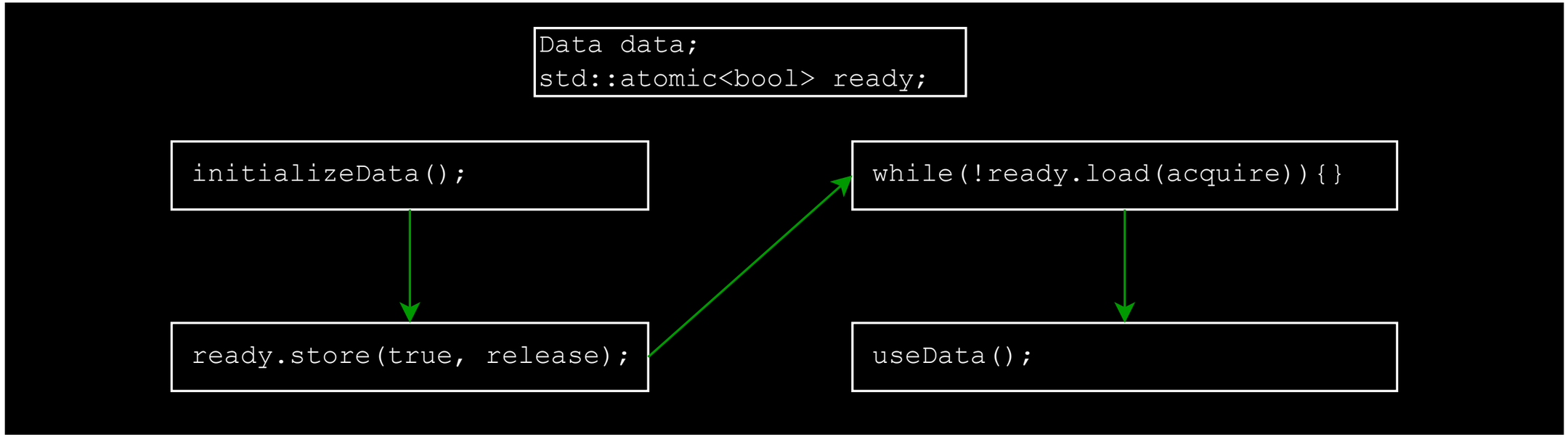

- Store happens-before load
- Can't reorder memory ops after the release-store
- Can't reorder memory ops before the acquire-load
- But opposite is ok

MULTI THREADED EXAMPLE (X86)

```
Data data;
std::atomic<bool> ready{false};

void producer()
{
    initializeData();
    ready.store(true, std::memory_order_releas
}

void consumer()
{
    while(!ready.load(std::memory_order_acquir
    useData();
}
```

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SQUAREHEAD TECHNOLOGY

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```

Also, `memory_order::`

- `acq_rel` (read-modify-write ops)
- `consume` (don't use)

How does the compiler know what is safe and not?

SQUAREHEAD
TECHNOLOGY

CPU MEMORY MODEL

SQUAREHEAD TECHNOLOGY

WHAT DO WE MEAN BY (RE)ORDERING?

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- Out of order micro-op execution?
- Pipeline?
- Forwarding networks?
- Store buffers?
- Store/load coalescing?
- Memory system?
- Caches?

SQUAREHEAD TECHNOLOGY

MEMORY (CONSISTENCY) MODEL

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SQUAREHEAD TECHNOLOGY

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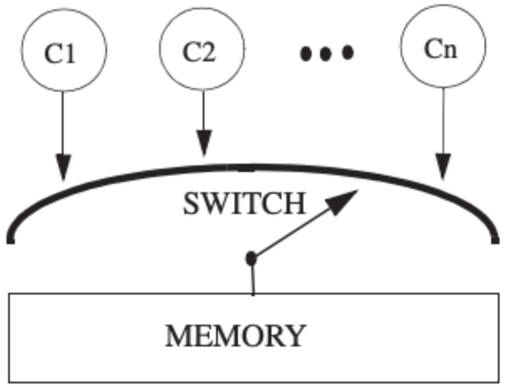

Sarin, Hill, Wood: A Primer on Memory Consistency and Cache Coherence

SQUAREHEAD TECHNOLOGY

PROGRAM ORDER

Producer thread

```
mov reg_0 42
store *data reg_0
mov reg_1 1
store *ready reg_1
```

PROGRAM ORDER

Producer thread

```
mov reg_0 42
store *data reg_0
mov reg_1 1
store *ready reg_1
```

Consumer thread

```
.wait
load reg_0 *ready
jz reg_0 .wait
load reg_1 *data
(use reg_1)
```

PROGRAM ORDER

Producer thread

```
store *data reg_0
store *ready reg_1
```

Consumer thread

```
load reg_0 *ready
load reg_1 *data
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PROGRAM ORDER

Producer thread	Consumer thread
`store *data reg_0`	`load reg_0 *ready`
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What is a valid order here?

PROGRAM ORDER

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- imagine each thread takes turns (as-if rule).

PROGRAM ORDER

Producer thread	Consumer thread
`store *data reg_0`	`load reg_0 *ready`
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What is a valid order here?

- In the (imaginary) global, total memory order,
- imagine each thread takes turns (as-if rule).
- How much of program order is preserved?

MEMORY ORDER

Producer thread

```
store *data reg_0
store *ready reg_1
```

Memory order

```
store *data reg_0
store *ready reg_1
load reg_0 *ready
load reg_1 *data
```

Consumer thread

```
load reg_0 *ready
load reg_1 *data
```

SQUAREHEAD TECHNOLOGY

MEMORY ORDER

Producer thread	Memory order	Consumer thread
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SQUAREHEAD TECHNOLOGY

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	`load reg_0 *ready`	
	`load reg_1 *data`	
	`store *data reg_0`	

SQUAREHEAD TECHNOLOGY

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Producer thread	Memory order	Consumer thread
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- Sequential consistency

SQUAREHEAD TECHNOLOGY

MEMORY ORDER

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Memory order

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- Sequential consistency
- All of program order is preserved

SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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- Sequential consistency
- All of program order is preserved
- Easy to reason about
- Less possibilities for optimization ("no-one" does this)

SEQUENTIAL CONSISTENCY

Preserves

- Load → Load
- Store → Store
- Load → Store
- Store → Load

TOTAL STORE ORDERING (TSO) (~X86)

Preserves

- Load → Load
- Store → Store
- Load → Store
- ~~Store → Load~~

TOTAL STORE ORDERING (TSO) (~X86)

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TOTAL STORE ORDERING (TSO) (~X86)

- Motivated by store buffers
- Stores are buffered on the core into a store buffer
- A later load might take its value before the buffer is drained to cache

TSO EXAMPLE

Thread 1	Thread 2
`store x 1`	`store y 1`
`load y`	`load x`

TSO EXAMPLE

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Can `x` *and* `y` be `0`?

SQUAREHEAD TECHNOLOGY

TSO EXAMPLE

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`store x 1`	`load y`	`store y 1`
`load y`	`store y 1`	`load x`
	`load x`	
	`store x 1`	

SQUAREHEAD TECHNOLOGY

TSO EXAMPLE

Thread 1	Memory order	Thread 2
`store x 1`	`load y`	`store y 1`
`load y`	`store y 1`	`load x`
	`load x`	
	`store x 1`	

`x == 0, y == 0`

Fine on TSO, not on SC!

CLARIFICATION

Thread 1

```
store x 1
```

```
load x
```

CLARIFICATION

Thread 1

```
store x 1
```

```
load x
```

Can `store x` be ordered after `load x`?

SQUAREHEAD TECHNOLOGY

CLARIFICATION

Thread 1	Memory order
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SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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SQUAREHEAD TECHNOLOGY

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RELAXED MEMORY MODELS (ARM, RISC-V)

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- What if want non-FIFO store buffers?
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- What if we want fancy speculation and prediction?
- What if we want other optimizations in the memory system / cache?

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS

Producer thread

```
store *data0 reg_0
store *data1 reg_1
store *ready reg_2
```

Consumer thread

```
load reg_0 *ready
load reg_1 *data0
load reg_2 *data1
```

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS

Producer thread

```
store *data0 reg_0
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```

Memory order

```
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store *ready reg_2
load reg_0 *ready
load reg_2 *data1
load reg_1 *data0
```

Consumer thread

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  - Give the architecture a lot of freedom to optimize
  - Tell it which memory operations I care about
  - At least a few safe defaults
  - A memory model to reason about

RELAXED MEMORY MODELS: RISC-V

SAFE DEFAULTS: SAME ADDRESS STORE → STORE

Producer thread

```
store *data0 reg_0
store *data0 reg_1
```

Memory order?

```
store *data0 reg_1
store *data0 reg_0
```

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS: RISC-V

SAFE DEFAULTS: DATA DEPENDENCY

Producer thread

```
load reg_0 *data0
store *data1 reg_0
```

Memory order?

```
store *data1 reg_0
load reg_0 *data0
```

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS: RISC-V

SAFE DEFAULTS: ADDRESS DEPENDENCY

Producer thread

```
load reg_0 pointer
store *reg_0 2
```

Memory order?

```
store *reg_0 2
load reg_0 pointer
```

RELAXED MEMORY MODELS: RISC-V

FENCES

Producer thread

```
store *data0 reg_0
store *data1 reg_1
store *ready reg_2
```

Memory order

```
store *data1 reg_1
store *data0 reg_0
store *ready reg_2
load reg_0 *ready
load reg_2 *data1
load reg_1 *data0
```

Consumer thread

```
load reg_0 *ready
load reg_1 *data0
load reg_2 *data1
```

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS: RISC-V

FENCES

Producer thread

```
store *data0 reg_0
store *data1 reg_1
fence w, w
store *ready reg_2
```

Memory order

```
store *data1 reg_1
store *data0 reg_0
store *ready reg_2
load reg_0 *ready
load reg_2 *data1
load reg_1 *data0
```

Consumer thread

```
load reg_0 *ready
fence r, r
load reg_1 *data0
load reg_2 *data1
```

SQUAREHEAD TECHNOLOGY

RELAXED MEMORY MODELS: RISC-V

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  - Don't reorder across fences (depending on type of fence)
  - Don't reorder across AMOs with acquire/release semantics
  - And more, see "Preserved Program Order" in RISC-V ISA manual

SQUAREHEAD
TECHNOLOGY

Language memory model

SQUAREHEAD TECHNOLOGY

Language memory model

↓

Architecture memory model

↓

Language memory model

↓

Architecture memory model

↓

Microarchitecture (pipeline, store buffers)

Language memory model

↓

Architecture memory model

↓

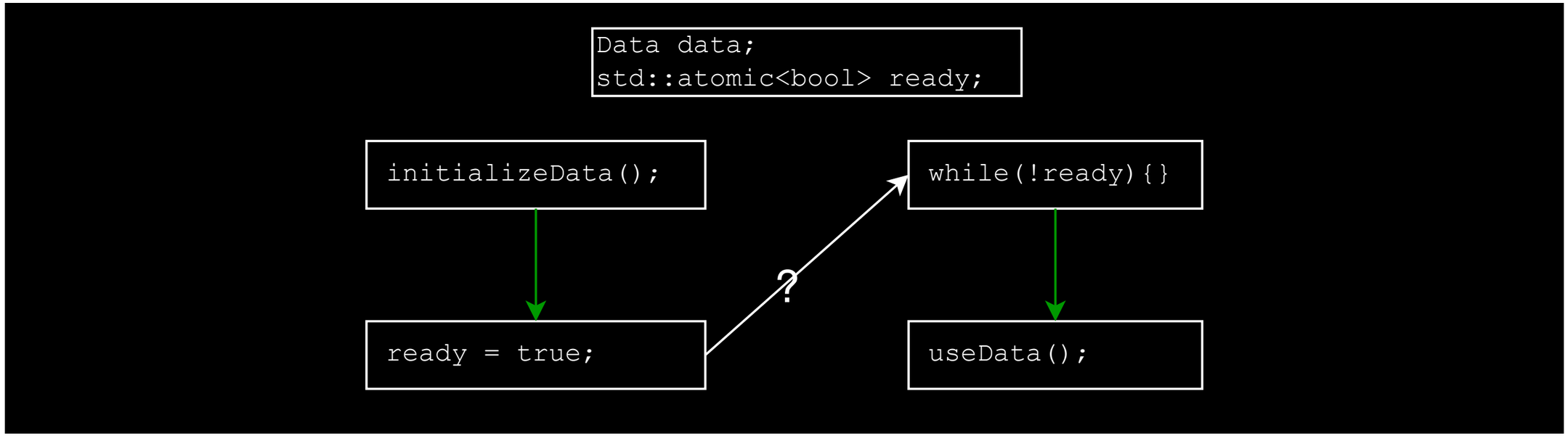
Microarchitecture (pipeline, store buffers) and cache coherence

SQUAREHEAD
TECHNOLOGY

REMEMBER

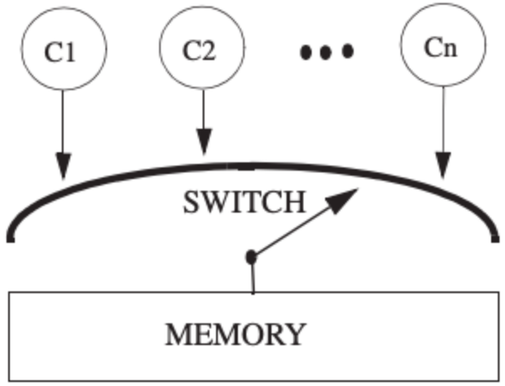
SQUAREHEAD TECHNOLOGY

C++ MEMORY MODEL



SQUAREHEAD TECHNOLOGY

CPU MEMORY MODEL



SQUAREHEAD TECHNOLOGY

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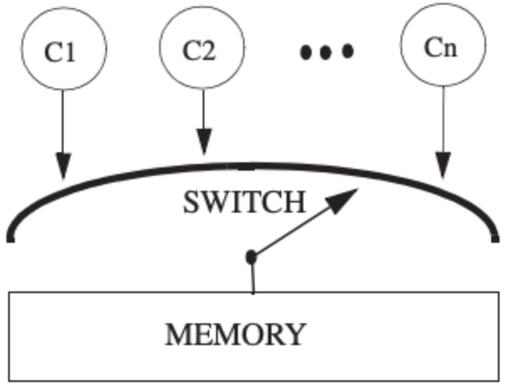

Producer thread

```
store *data reg_0
store *ready reg_1
```

Memory order

```
store *data reg_0
store *ready reg_1
load reg_0 *ready
load reg_1 *data
```

Consumer thread

```
load reg_0 *ready
load reg_1 *data
```

SQUAREHEAD
TECHNOLOGY

BONUS!

DON'T TRUST THE ASSEMBLY

SQUAREHEAD TECHNOLOGY

THE TWO MEMORY MODELS

ANDERS SCHAU KNATTEN

C++ UNDER THE SEA 2025

Squarehead / CppQuiz.org